# ECE2372 – Modern Digital System Design

Spring 2024

Department of Electrical and Computer Engineering, Texas Tech University

**Instructor:** Dr. Kai Wu
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**Class Meeting Time:** Tue, Thu 2:00 PM ~ 3:20 PM
**Classroom:** Electrical Engineering 217
**Office Hours:** Tue, Thu 3:30 PM ~ 4:30 PM, or by appointment
**Class Website:** *Blackboard*
**Grader:** Shivakrishna Erroju (serroju@ttu.edu). Mon, Thu, 5:00 PM ~ 6:00 PM. Electrical Engineering 218.
**Tutor**: Aidan Singh (aisingh@ttu.edu). Mon, Wed, Thu, 5:00 PM ~ 7:30 PM. Electrical Engineering 218.
Logan House (loghouse@ttu.edu). Mon, Wed, Fri, 9:30 AM ~ 11:00 AM. Electrical Engineering 218A.
**Supplemental Instruction (SI) Leader:** Justin Bayley (jubayley@ttu.edu). Mon, Wed, 7:00 PM ~ 8:30 PM. Holden Hall 038

**Required Textbooks:**

- M.M. Mano and C.R. Kime, *Logic and Computer Design Fundamentals*, 4th or 5th Edition, Pearson - Prentice Hall.

**Expected Learning Outcomes**

Upon completion of this course, students will be able to:

- Analyze and design combinational digital logic circuits.
- Analyze and design sequential digital logic circuits.
- Use hardware description language.

**ABET Student Learning Outcomes Addressed**

1. An ability to identify, formulate, and solve complex engineering problems by applying engineering, science, and mathematics principles.
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.
3. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

**Methods of Assessment of Learning Outcomes**

The learning outcome will be evaluated based on students' performance in homework and exams (fundamental knowledge) and design projects (practical skills).

**Grading:**

- Homework/Quizzes: 16%
- In-class exams (two exams counted at 24% each): 48%
- Final exam: 20%
- Projects: 16%

**Approximate Final Grade Evaluation:**

- A+: ≥ 97
- A: 96 - 90
- B: 89 - 80
- C: 79 - 70
- D: 69 - 60
- F: < 60

**In-Class Exam Policy:**

Three in-class exams (80 minutes each) will be offered. The two with the highest scores will be automatically counted into a student's grade. Students can skip the last in-class makeup exam) if he/she is satisfied with the

previous two. Refer to 'Preliminary Course Schedule' for tentative exam dates. (Note: the final exam is mandatory for every student)

**Preliminary Course Outline (subject to changes)**

1 Number systems
2 Boolean algebra, Karnaugh maps, simplifications
3 Logic circuits, gates, basic logic implementation
4 Combinational logic design and implementation
5 Hardware description languages
6 Basic cell, flip-flop design, timing consideration
7 Sequential circuit analysis and design (state assignment, next state, and output decoders), counter design
8 Hardware description language for sequential design
9 Registers and counters
10 Memory and programmable devices

**Subject Matter for Each Lecture**
(Note: the schedule is subject to changes and will be updated throughout the semester)

| Tuesday | Thursday |
|---|---|
| **January** | |
| | 1/11: Introduction, number system |
| 1/16: Arithmetic operations, base conversion | 1/18: Arithmetic operations, base conversion |
| 1/23: Arithmetic operations, base conversion | 1/25: Gates and Boolean equations |
| 1/30: Gates and Boolean equations | |
| **February** | |
| | 2/1: Standard forms, optimization, K-map |
| 2/6: Standard forms, optimization, K-map | 2/8: K-map continue, additional gates |
| 2/13: Exam 1 Review, Combinational logic design procedure | 2/15: Exam #1 |
| 2/20: EDA tutorial | 2/22: Combinational logic |
| 2/27: Binary adder, binary subtraction | 2/29: Binary adder, binary subtraction |
| **March** | |
| | |
| 3/5: Other arithmetic functions | 3/7: Hardware tutorial |
| 3/12: Spring Break (no class) | 3/14: Spring Break (no class) |
| 3/19: Project discussion | 3/21: Exam #2 Review, Storage elements |
| 3/26: Exam #2 | 3/28: Storage elements |
| **April** | |
| 4/2: Sequential circuit analysis | 4/4: Sequential circuit design |
| 4/9: State machine design | 4/11: State machine design |
| 4/16: CMOS, programmable devices | 4/18: Exam #3 review |
| 4/23: Exam #3 (makeup exam) | 4/25: Final review |
| 4/30: Last day of class (Office Hour) | |
| | |
| **Final Exam: Monday, May 6th, 4:30 pm – 7:00 pm** | |

**Academic Honesty**

*Academic integrity is taking responsibility for one's own class and/or course work, being individually accountable, and demonstrating intellectual honesty and ethical behavior. Academic integrity is a personal choice to abide by the standards of intellectual honesty and responsibility. Because education is a shared effort to achieve learning through the exchange of ideas, students, faculty, and staff have the collective responsibility to build mutual trust and respect. Ethical behavior and independent thought are essential for the highest level of academic achievement, which then must be measured. Academic achievement includes scholarship, teaching, and learning, all of which are shared endeavors. Grades are a device used to quantify the successful accumulation of knowledge through learning. Adhering to the standards of academic integrity ensures grades are earned honestly. Academic integrity is the foundation upon which students, faculty, and staff build their educational and*

*professional careers. [Texas Tech University ("University") Quality Enhancement Plan, Academic Integrity Task Force, 2010.*

**Accommodations for Students with Disabilities**

*Any student who, because of a disability, may require special arrangements to meet the course requirements should contact the instructor as soon as possible to make any necessary arrangements. Students should present appropriate verification from Student Disability Services during the instructor's office hours. Please note instructors are not allowed to provide classroom accommodations to a student until appropriate verification from Student Disability Services has been provided. For additional information, please contact Student Disability Services in West Hall or call 806-742-2405.*

**Religious Holiday**

*"Religious holy day" means a holy day observed by a religion whose places of worship are exempt from property taxation under Texas Tax Code §11.20. A student who intends to observe a religious holy day should make that intention known in writing to the instructor before the absence. A student who is absent from classes for the observance of a religious holy day shall be allowed to take an examination or complete an assignment scheduled for that day within a reasonable time after the absence. A student who is excused under section 2 may not be penalized for the absence; however, the instructor may respond appropriately if the student fails to complete the assignment satisfactorily.*